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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/530,661	09/20/1995	BRENT KEETH	2269-5990US (95-0424.00/U)	5492
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EXAMINER MONTALVO, EVA Y				
ART UNIT 2814		PAPER NUMBER		
NOTIFICATION DATE 04/09/2009		DELIVERY MODE ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary

Application No.

08/530,661

Applicant(s)

KEETH ET AL.

Examiner

Eva Montalvo

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 December 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 28-31, 34-47 is/are pending in the application.
- 4a) Of the above claim(s) 37-47 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 28-31 and 34-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/C)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date 12/17/2008, 2/17/2009

DETAILED ACTION

1. This Office action responds to the election filed on 12/17/2008.

Acknowledgement

2. The Amendment filed on 12/17/2008, responding to the Office action mailed on 09/18/2008, has been entered into the record. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this office action are claims 28-31, 34-47, with claims 37-47 withdrawn from consideration in the previous action.

Specification

3. The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 28, 29, 31 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison in view of Chin (cited in previous action).

Dennison discloses an integrated circuit (see Fig. 10) comprising a semiconductor die (10); a plurality of memory cells arranged in at least one array formed on the semiconductor die, each of the plurality of memory cells including at least one container-configured capacitor (72) having a storage node (62) including a roughened outer surface in a substantially vertical dimension with respect to the semiconductor die (see col. 3, lines 25-49); a word line (14) formed substantially below the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the word line; and a first digit line (94) formed substantially above the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the first digit line (see col. 7, lines 4-9).

Although the device disclosed by Dennison shows substantial features of the claimed invention, it fails to expressly a device, further comprising a second digit line, where the second digit line and the first digit line are separated by an insulated dielectric material.

Nonetheless, these features are well known in the art and would have been an obvious modification of the device disclosed by Dennison, as evidenced by Chin. Chin discloses a device, comprising a second digit line (22) formed substantially above the first digit line, where

the second digit line and the first digit line are separated by an insulated dielectric material (see Fig. 3).

Given the teachings of Chin, a person having ordinary skill in the art at the time of invention would have readily recognized the desirability and advantages of modifying Dennison, as suggested by Chin, by employing a dielectric layer between the first and second digit lines. This cell arrangement would produce a wide effective area for the capacitor and improve the topology of the digit line contact area (Chin: col. 4, lines 59-68 and col. 5, lines 1-10).

As to claim 29, Dennison discloses an integrated circuit with memory cells, but fail to expressly teach circuitry formed on the semiconductor die and coupled to the memory cells for permitting data to be written to and read from the plurality of memory cells. However, it is well known in the art that additional circuitry coupled to the memory cell is needed to operate the DRAM cell. Furthermore, Dennison's device would not be functional or operable without additional control circuitry coupled to the memory cell.

In reference to the language referring to the function of the semiconductor device, i.e., for permitting data to be written to and read from the plurality of memory cells, intended use and other types of functional language must result in a structure difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In *re Casey*, 152 USPQ 235 (CCPA 1967); In *re Otto*, 136 USPQ 458, 459 (CCPA 1963); *Ex Parte Masham*, 2USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). In the instant case and as explained above, Dennison implicitly teaches all structure limitations specifically recited in the claim and since permitting data to be written to and read from the memory cells involves a mere

manipulation of the applied current it appears that the recited functional limitation does not affect the structure of Dennison's device.

As to claims 31 and 34, Dennison discloses a circuit further comprising a conductive isolation line (19, see Fig. 1) formed substantially below the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the conductive isolation line; and where the memory cells are dynamic random access memory cells (see Fig. 10).

7. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison in view of Chin, as applied to claim 28 above, and further in view of Takashima (cited in previous action).

Although the device disclosed by Dennison in view of Chin shows substantial features of the claimed invention, it fails to expressly a device, where the memory cells are formed with a minimum capable photolithographic feature dimension, and a single one of the memory cells consumes an area of no more than eight times the square of the minimum capable photolithographic feature dimension.

Nonetheless, these features are well known in the art and would have been an obvious modification of the device disclosed by Dennison in view of Chin, as evidenced by Takashima.

Takashima discloses a DRAM device, where the memory cells are formed with a minimum capable photolithographic feature dimension, and a single one of the memory cells consumes an area of no more than eight times the square of the minimum capable photolithographic feature dimension (col. 5, lines 20-30 and col. 25, lines 17-20).

Given the teachings of Takashima, a person having ordinary skill in the art at the time of invention would have readily recognized the desirability and advantages of modifying Dennison

in view of Chin, as suggested by Takashima, by constructing a DRAM cell to a size of $6F^2$. This cell arrangement would enable a trench type of memory cell where random access can be made and noise is small (col. 25 lines 17-19).

8. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison in view of Chin, as applied to claim 28 above and further in view of Eimori (cited in the previous actions).

Chin discloses a device where at least where at least 16,000,000 to 17,000,000 functional and operably addressable memory cells are formed on the semiconductor die (see col. 1, lines 58-60) and cell area of 80 mm^2 (5 um^2).

Although the prior art does not show the claimed cell area of less than 14 mm^2 , absent any criticality, this is only considered to be the "optimum" values, and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as the design rules of the memory cells decreases, as already suggested by Chin (see col. 1, lines 14-17). In addition, Eimore discloses a DRAM where a design rule of 0.25 micron (see col. 4, lines 25-31) would lead to a combine area of 16M memory cells to less than 6 mm^2 .

Furthermore, the specification fails to provide teachings about the criticality of having a specific area for the memory cells. It has been held that area difference will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such distance range is critical. "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Since the applicants have not established the criticality (see paragraph 9) of the area claimed, it would have been obvious to one of ordinary skill in the art to use the value in the method of Eimore.

CRITICALITY

9. The specification contains no disclosure of either the critical nature of the claimed memory cell area or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

10. Applicant's arguments filed 12/17/2008 have been fully considered but they are not persuasive

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Montalvo whose telephone number is (571)270-3829. The examiner can normally be reached on Monday through Thursday 7:30-5:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marcos D. Pizarro-Crespo can be reached on (571)272-1716. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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